Claim Amendments

1. (As Issued) An apparatus, comprising:

an integrated system management memory region; and

a system management interrupt address decode unit to fetch instructions from the integrated system management memory region in response to a system management interrupt acknowledge signal asserted by a processor, the system management interrupt decode unit to fetch instructions from the integrated system management memory region regardless of a system management interrupt address received from the processor.

2. (As Issued) The apparatus of claim 1, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

3. (As Issued) The apparatus of claim 2, wherein the system management interrupt address is the first address received following the assertion of the system management interrupt acknowledge signal by the processor.

4. (As Issued) The apparatus of claim 3, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

5. (As Issued) The apparatus of claim 4, the system management interrupt address decode unit to fetch system management interrupt handler instructions stored in a system main memory in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.

6. (As Issued) The apparatus of claim 5, wherein the system management interrupt handler instructions stored in the system main memory are part of a basis input/output system (BIOS).

7. (As Issued) The apparatus of claim 6, wherein the integrated system management memory region is at least 128 bytes in size.

8. (As Issued) A method, comprising:

receiving a system management interrupt acknowledge signal from a processor; and

fetching a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller regardless of a system management memory address indicated by the processor in response to the system management interrupt acknowledge signal.

9. (As Issued) The method of claim 8, further comprising latching the system management memory address indicated by the processor.

10. (As Issued) The method of claim 9, wherein latching the system management memory address includes latching a first address delivered by the processor following receiving the system management interrupt acknowledge signal.

11. (As Issued) The method of claim 10, further comprising comparing a plurality of addresses received from the processor with the latched address.

12. (As Issued) The method of claim 11, further comprising fetching a plurality of system management interrupt handler instructions from a section of BIOS code in a system main memory if comparing a plurality of addresses received from the processor with the latched address results in a match.

13. (As Issued) A system, comprising:

a processor;

a system main memory; and

a memory controller coupled between the processor and the system main memory, the memory controller including

an integrated system management memory region, and

a system management interrupt address decode unit to fetch instructions from the integrated system management memory region in response to a system management interrupt acknowledge signal asserted by the processor, the system management interrupt decode unit to fetch instructions from the integrated system management memory region regardless of a system management interrupt address received from the processor.

14. (As Issued) The system of claim 13, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

15. (As Issued) The system of claim 14, wherein the system management interrupt address is the first address received by the memory controller following the assertion of the system management interrupt acknowledge signal by the processor.

16. (As Issued) The system of claim 15, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

17. (As Issued) The system of claim 16, the system management interrupt address decode unit to fetch system management interrupt handler instructions stored in the system main memory in response to the compare unit finding a match between

the latched system management interrupt address and one of the plurality of addresses received from the processor.

18. (As Issued) The system of claim 17, wherein the system management interrupt handler instructions stored in the system main memory are part of a basis input/output system (BIOS).

19. (As Issued) The system of claim 18, wherein the integrated system management memory region is at least 128 bytes in size.

20. (New) An apparatus, comprising:

a system management memory; and

a system management interrupt address decode unit to fetch instructions from the system management memory in response to a system management interrupt acknowledge signal asserted by a processor, the system management interrupt decode unit to fetch instructions from the system management memory regardless of a system management interrupt address received from the processor.

21. (New) The apparatus of claim 20, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

22. (New) The apparatus of claim 21, wherein the system management interrupt address is the first address received following the assertion of the system management interrupt acknowledge signal by the processor.

23. (New) The apparatus of claim 22, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

24. (New) The apparatus of claim 23, wherein the system management interrupt address decode unit fetches system management interrupt handler instructions stored in a system main memory in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.

25. (New) The apparatus of claim 24, wherein the system management interrupt handler instructions stored in the system main memory are part of a basic input/output system (BIOS).

26. (New) A method, comprising:

receiving a system management interrupt acknowledge signal from a processor; and

in response to the system management interrupt acknowledge signal, fetching a plurality of system management interrupt handler instructions from a system management memory instead fetching a plurality of system management interrupt handler instructions of a basic input/output system (BIOS) identified by a system management memory address regardless of the system management memory address indicated by the processor.

27. (New) The method of claim 26, further comprising latching the system management memory address indicated by the processor.

28. (New) The method of claim 27, further comprising

comparing a plurality of addresses received from the processor with the latched address, and

fetching a plurality of system management interrupt handler instructions from the BIOS in response to the latched address matching an address of the a plurality of addresses received from the processor.

29. (New) The method of claim 26, further comprising fetching a plurality of system management interrupt handler instructions from the BIOS in response to the system management memory address matching an address of another]system management memory address previously received from the processor.

30. (New) A system, comprising:

a processor;

a system management memory,

a basic input/output system, and

a system management interrupt address decode unit to fetch instructions from the system management memory in response to a system management interrupt acknowledge signal asserted by the processor, the system management interrupt address decode unit to fetch instructions from the system management memory instead of fetching instructions of the basic input/output system identified by a system management interrupt address regardless of a system management interrupt address received from the processor.

31. (New) The system of claim 30, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

32. (New) The system of claim 31, wherein the system management interrupt address is the first received address received by the system management interrupt

decode unit following the assertion of the system management interrupt acknowledge signal by the processor.

33. (New) The system of claim 32, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

34. (New) The system of claim 33, wherein the system management interrupt address decode unit fetches system management interrupt handler instructions of the BIOS in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.